

DATA SHEET

TEA1400; TEA1400T High voltage smart power battery charge IC

Preliminary specification
Supersedes data of November 1991
File under Integrated Circuits, IC03

1995 Sep 26

High voltage smart power battery charge IC

TEA1400; TEA1400T

FEATURES

- Integrated 750 V / 0.5 A power sense FET
- Wide input voltage range of 9 to 650 V dc
- Current and voltage control functions
- High and low level current modes at V_{in} is 90 to 290 V ac
- Low level current mode control at V_{in} 12 to 24 V dc
- Undervoltage lock-out
- Cycle by cycle protection
- Thermal shutdown
- LED driver for mode indication.

GENERAL DESCRIPTION

The TEA1400 is a high voltage integrated circuit intended to perform the control and power switching functions in non isolated NiCd and NiMH battery charging systems. Moreover, the TEA1400 is designed to be used as a high performance switching regulator for compact power supplies, e.g. for mains isolated battery charger systems. The TEA1400's input voltage range is 9 V dc to 650 V dc. This range comprises not only the world wide mains, but also all car and truck batteries. The TEA1400 is designed in the so-called BCD Power Logic 750 process, including a 750 V open drain power sense FET with a sinking capability of 0.5 A.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	CODE
TEA1400	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT 38-1
TEA1400T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

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BLOCK DIAGRAM

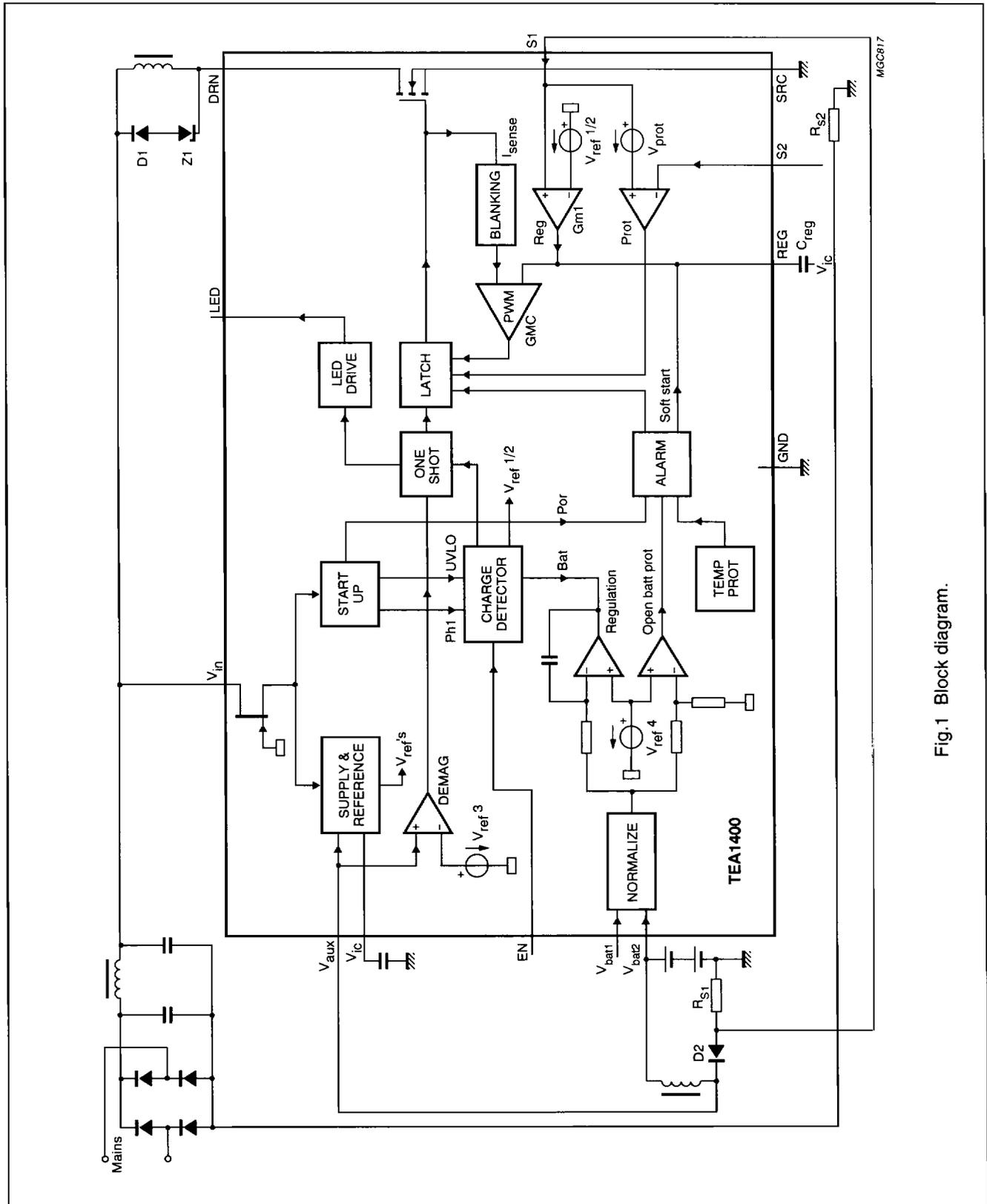


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN		DESCRIPTION
	SO20	DIP16	
V_{in}	1	1	input supply voltage
n.c.	2 to 4	2	not connected
n.c.	5	3	not connected
V_{bat1}	6	4	battery voltage sense at one cell
V_{bat2}	7	5	battery voltage sense at two cells
LED	8	6	power source interface signal/LED drive
EN	9	7	charge mode enable input
REG	10	8	loop control/soft start capacitor
GND	11	9	ground
S1	12	10	primary and/or charge current sense input
S2	13	11	primary protection current sense input
V_{ic}	14	12	IC supply
SRC	15	13	DMOS source
V_{aux}	16	14	take over supply voltage input
n.c.	17 to 19	15	not connected
DRN	20	16	DMOS drain

